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A Novel Pseudo-Differential Integer/ Fractional-Order Voltage-Mode All-Pass Filter

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***Abstract*—The paper presents the first- (integer) and fractional-order case studies of a novel pseudo-differential (P-D) voltage-mode all-pass filter (APF) employing a single differential voltage current conveyor (DVCC), one resistor, and a single grounded capacitor. The proposed filter brings significant reduction of complexity in comparison to available fully-differential or P-D filter topologies. Moreover, it was also shown that fractional-order capacitor can be used for gain response compensation of the proposed APF. The theoretical results of 0.8th and 1st-order APF were verified by Cadence IC6 Spectre simulations using new structure of DVCC via TSMC 0.18 µm CMOS process parameters supplied with ±0.9 V voltages.**

Keywords—all-pass filter; differential voltage current conveyor; DVCC; fractional-order capacitor; fractional-order filter; pseudo-differential filter; voltage-mode

I. INTRODUCTION

Fully-differential (F-D) first-(integer)-order all-pass filters (APFs) employing current conveyors (CCs) are advantageous in signal processing due to high performance benefits of CCs such as high accuracy, wide bandwidth, and exceptionally high slew rates combined with low-voltage and low-power implementations [1]. Particularly, APFs provide phase shifting while keeping the amplitude of input signal constant over the frequency range of interest, whereas F-D filters are attractive for industrial and wireless applications because of their high common mode rejection ratios for rejecting external interference [2]–[5]. In this regard, voltage-mode (VM) circuit topologies [6]–[8] worth to mention. However, common disadvantage of each solution is the use of excessive number of passive components mainly in floating form. This drawback can be overcome by so-called pseudo-differential (P-D) filter design technique [9]–[11]. Note that the resulting filter still features with differential input and output voltages. However, do not feature a F-D inner structure as it is the case of true-differential circuits. On the other hand, the inner structure of the circuit remains single-ended and less complex. Our brief literature survey showed that the available P-D first-order APFs in open literature [12]–[14] do not employ canonic number of active and passive components, i.e. singe device and one capacitor and resistor. Therefore, this paper aims (i) to introduce the least complex P-D first-order VM APF in canonic form, which is composed of one differential voltage current conveyor (DVCC), one resistor, and a grounded capacitor and (ii) presents both integer- and fractional-order (FO) case studies of the proposed filter. Cadence IC6 Spectre simulation results are included to prove the presented theory and the workability of the proposed filter.

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II. CIRCUIT DESCRIPTION

A. Differential Voltage Current Conveyor (DVCC)

The DVCC, which circuit symbol is depicted in Fig. 1 (a), is a four-terminal device [15] with one low-impedance current input X, two high-impedance voltage inputs $Y_{1,2}$ and a high-impedance current output Z. Using a standard notation and taking into account main parasitics of DVCC given in Fig. 1(b), it can be described by the following hybrid matrix:

$$\begin{bmatrix} I_{Y1} \\ I_{Y2} \\ V_X \\ I_Z \end{bmatrix} = \begin{bmatrix} Y_{Y1}(s) & 0 & 0 & 0 \\ 0 & Y_{Y2}(s) & 0 & 0 \\ \beta_1(s) & -\beta_2(s) & Z_X & 0 \\ 0 & 0 & \gamma(s) & Y_Z(s) \end{bmatrix} \begin{bmatrix} V_{Y1} \\ V_{Y2} \\ I_X \\ V_Z \end{bmatrix}, \quad (1)$$

where $Z_X = R_X$ is a non-zero parasitic intrinsic input impedance at X terminal and $Y_k = sC_k + 1/R_k$ for $k = \{Y_1, Y_2, Z\}$ are parasitic admittances appear between the corresponding high-impedance input or output terminals of DVCC, respectively, and ground. In (1), parameters $\gamma(s)$ and $\beta_j(s)$ for $j = \{1, 2\}$ represent frequency-dependent non-ideal current and voltage gains, respectively. Note that using single-pole model they can be defined as $\gamma(s) = \gamma_o/(1 + s\tau_\gamma)$ and $\beta_j(s) = \beta_{oj}/(1 + s\tau_{\beta j})$. Here, γ_o and β_{oj} are DC current and voltage gains and $1/\tau_\gamma$ and $1/\tau_{\beta j}$ are bandwidths in order of a few Grad/s that dependent on the IC fabrication of the active device. However, at low and medium frequencies, i.e. $f \ll [(2\pi)^{-1}] \times \min\{1/\tau_\gamma, 1/\tau_{\beta j}\}$, the frequency-dependent gains turn to $\gamma(s) \cong \gamma_o = 1 - \varepsilon_{\gamma i}$ and $\beta_j(s) \cong \beta_{0j} = 1 - \varepsilon_{\beta jv}$, where $\varepsilon_{\gamma i}$ and $\varepsilon_{\beta jv}$ denote the current and

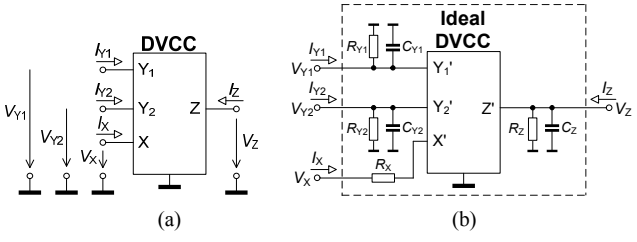

Fig. 1. DVCC: (a) circuit symbol, (b) its main parasitic components.

voltage tracking errors and satisfy $|\varepsilon_{\gamma i}| \ll 1$ and $|\varepsilon_{\beta jv}| \ll 1$. Ideally, the DC non-ideal gains are equal to unity, i.e. $\gamma_o = 1$, $\beta_{oj} = 1$ and their bandwidths are equal to infinity.

B. First-(Integer)-Order VM APF Design

The proposed new P-D first-(integer)-order VM APF using single DVCC, one resistor, and a single capacitor is shown in Fig. 2(a). Unity-gain voltage buffers (VBs) are used to prevent the loading effect. Considering an ideal DVCC, routine circuit analysis yields the following voltage transfer function (TF) in differential mode:

$$A_{\rm dm}(s) = \frac{V_{\rm o1} - V_{\rm o2}}{V_{\rm i1} - V_{\rm i2}} = \frac{V_{\rm od}}{V_{\rm id}} = \frac{1}{2}\left(\frac{2 - sCR}{2 + sCR}\right), \qquad (2)$$

which indicates a TF of first-order APF with non-inverting response and its pass-band gain at $\omega = 0$ is +1/2. From (2) the resulting zero (ω_z) and pole (ω_p) frequencies are as follows $\omega_z = \omega_p = 2/CR$ and their sensitivities to passive elements are unity in relative magnitude $S_{C,R}^{\omega_p,\omega_z} = -1$. Hence, the proposed filter shows low sensitivity performance. The phase response of the filter is found as $\varphi(\omega) = -2\tan^{-1}(\omega CR/2)$. Therefore, the phase of the filter varies from 0 (at $\omega = 0$) to $-\pi$ (at $\omega = \infty$).

For a complete circuit analysis it is important to consider the real behavior of DVCC described in (1) and VBs. Hence, for the proposed P-D first-order VM APF including the relevant parasitics in Fig. 2(b) it is important to take into account the effects of DC current γ_o and voltage β_{oj} gains, the non-zero parasitic intrinsic input resistance R_X at X terminal, and finite output admittance $Y_Z = sC_Z + 1/R_Z$ at Z terminal of DVCC. On the other hand, parasitic admittances at terminals Y_1 and Y_2 can be neglected due to their connection to input voltage sources. Note that R_X is connected in series with external resistor R and the parasitic capacitance C_Z appears in parallel with external capacitor C. Hence, in further analysis the total resistance and capacitance at nodes ① and ② can be considered respectively as $R' = R + R_X$ and $C' = C + C_Z$, while $Z_Z = R_Z$. Therefore, the ideal TF in (2) converts to:

$$A'_{\rm dm}(s) = \frac{1}{2}\left[\frac{Z_Z(\gamma_o + 1)\left[\beta_{o3}(\beta_{o1} + \beta_{o2}) - \beta_{o4}\right] - \beta_{o4}R'(1 + sC'Z_Z)}{Z_Z(\gamma_o + 1) + R'(1 + sC'Z_Z)}\right]. \qquad (3)$$

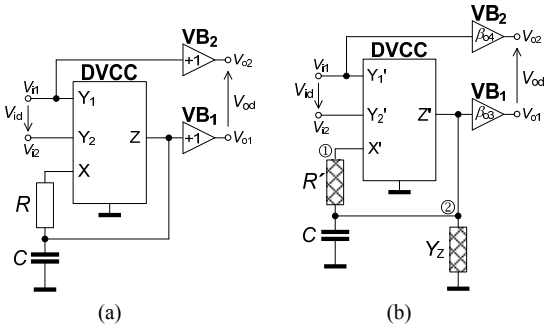

Fig. 2. Proposed pseudo-differential VM APF: (a) ideal circuit, (b) including the relevant parasitic components and non-ideal gains.

TABLE I. DESIGN PARAMETERS OF AN IDEAL P-D FO VM APF.

$\lvert A_{{\rm dm},\alpha}(\omega)\rvert$ (a)	$\frac{1}{2}\sqrt{\frac{4 - 4\omega^\alpha C_\alpha R\cos(\alpha\pi/2) + (\omega^\alpha C_\alpha R)^2}{4 + 4\omega^\alpha C_\alpha R\cos(\alpha\pi/2) + (\omega^\alpha C_\alpha R)^2}}$
$\varphi_\alpha(\omega)$ (b)	$-\tan^{-1}\left[\frac{\omega^\alpha C_\alpha R\sin(\alpha\pi/2)}{2 - \omega^\alpha C_\alpha R\cos(\alpha\pi/2)}\right] - \tan^{-1}\left[\frac{\omega^\alpha C_\alpha R\sin(\alpha\pi/2)}{2 + \omega^\alpha C_\alpha R\cos(\alpha\pi/2)}\right]$
$\omega_{z,\alpha}$ (c)	$\left\{2\left[\cos(\alpha\pi/2) + \sqrt{\cos(\alpha\pi/2)^2 - 1}\right]\Big/ C_\alpha R\right\}^{1/\alpha}$
$\omega_{p,\alpha}$ (d)	$\left\{-2\left[\cos(\alpha\pi/2) + \sqrt{\cos(\alpha\pi/2)^2 - 1}\right]\Big/ C_\alpha R\right\}^{1/\alpha}$

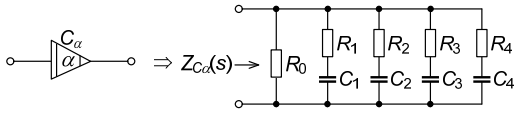

Fig. 3. RC network realization of fractional-order capacitor C_α [21].

Subsequently, it can be seen that ω'_z and ω'_p frequencies differ and can be given as:

$$\omega'_z = \frac{\frac{(\gamma_o + 1)\left[\beta_{o3}(\beta_{o1} + \beta_{o2}) - \beta_{o4}\right]}{\beta_{o4}} - \frac{R'}{Z_Z}}{C'R'}, \omega'_p = \frac{\gamma_o + 1 + \frac{R'}{Z_Z}}{C'R'}. \qquad (4)$$

Here it is worth noting that the affect of parasitic components and non-idealities of DVCC on (3) and (4) can be significantly minimized by proper selection of external passive components and/or by precise design of the used device.

C. Fractional-(Non-Integer)-Order VM APF Design

Considering the proposed P-D VM APF shown in Fig. 2(a) employing an ideal DVCC and VBs and assuming replacement of capacitor C of $\alpha = 1$ by a fractional-order capacitor (FoC) with pseudo-capacitance C_α $(0 < \alpha < 1)$ of impedance $Z_{C\alpha}(s) = 1/C_\alpha s^\alpha$ [16]–[20], the TF in (2) turns to:

$$A_{{\rm dm},\alpha}(s) = \frac{V_{\rm o1} - V_{\rm o2}}{V_{\rm i1} - V_{\rm i2}} = \frac{V_{\rm od}}{V_{\rm id}} = \frac{1}{2}\left(\frac{2 - s^\alpha RC_\alpha}{2 + s^\alpha RC_\alpha}\right), \qquad (5)$$

where the magnitude, phase, $\omega_{z,\alpha}$ and $\omega_{p,\alpha}$ frequencies are evaluated by replacement of s^α by $\omega^\alpha[\cos(\alpha\pi/2) + j\sin(\alpha\pi/2)]$ and C_α can be emulated via Foster II RC network shown in Fig. 3. The resulted design parameters of P-D VM APF in fractional domain are given in Table I.

Now, applying an identical non-ideal study on the proposed P-D VM APF, i.e. in Fig. 2(b) considering effects of DC gains and $R' = R + R_X$, the ideal FO TF in (5) converts to:

$$A'_{{\rm dm},\alpha}(s) = \frac{1}{2}\left[\frac{(\gamma_o + 1)\left[\beta_{o3}(\beta_{o1} + \beta_{o2}) - \beta_{o4}\right] - \beta_{o4}R'(Y_Z + s^\alpha C_\alpha)}{\gamma_o + 1 + R'(Y_Z + s^\alpha C_\alpha)}\right]. \qquad (6)$$

It is important to note that the finite output admittance Y_Z appearing between the node ② and ground has an integer-order character and must be assumed as $sC_Z + 1/R_Z$ due to difference in capacitances of C_α and C_Z from their nature (see [22]).

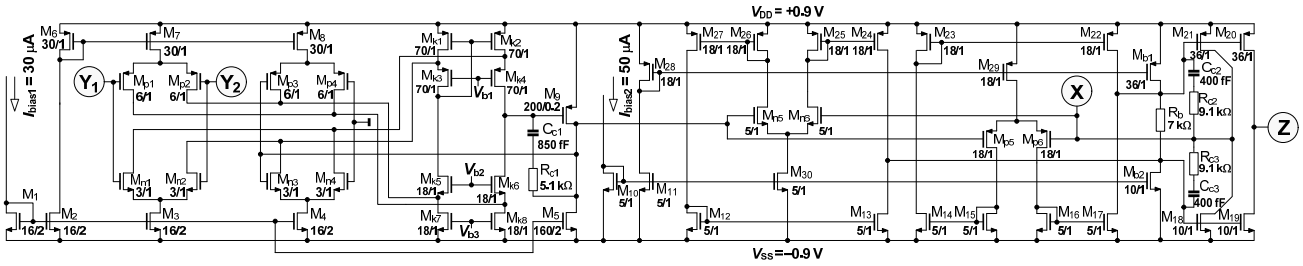

Fig. 4. CMOS implementation of DVCC based on 0.18 µm TSMC technology.

III. Simulation Results

To verify the theoretical analysis, firstly the behavior of the newly designed CMOS implementation of DVCC shown in Fig. 4 has been verified by simulations in Cadence IC6 Spectre analog design environment. Particularly, the internal structure of the DVCC, which is under fabrication in EUROPRACTICE IC Service, consists of two sub-blocks. The input stage is formed by differential difference amplifier (DDA) with internal feedback loop [23], which provides the input voltage difference operation $V_X = V_{Y1} - V_{Y2}$. The core of the second stage is realized by class AB non-inverting positive-type second-generation current conveyor (CCII+) [24]. DC power supply voltages equal to $+V_{DD} = -V_{SS} = 0.9$ V were used in design and transistors were modeled by the TSMC 0.18 µm CMOS process parameters available in EUROPRACTICE IC Service design kit. The achieved quiescent total power dissipation of the proposed device is 2.38 mW. The CMOS DVCC uses two types of transistors with following parameters (for width » length): typical ($V_{thP} = 0.48$ V, $K_{pP} = 39$ µA/V^2; $V_{thN} = 0.47$ V, $K_{pN} = 148$ µA/V^2) and medium threshold voltage type ($V_{thP} = 0.2$ V, $K_{pP} = 53$ µA/V^2; $V_{thN} = 0.29$ V, $K_{pN} = 180$ µA/V^2). Presented design, values of aspect ratios (W/L), and other parameters in CMOS implementation suppose trade-off between power consumption, dynamics, linearity, and –3 dB frequencies up to 100 MHz.

A. Small-Signal Parameters of DVCC

One of the main source of non-idealities and the most important small-signal parameter of the designed DVCC is non-zero parasitic intrinsic input resistance R_X at X terminal. Its value showed large dispersion in corner analysis (24 to 44) Ω, while the effects in Monte Carlo and temperature analyses (–25 to 50 °C) are insignificant and its value remains very close to nominal one (31 to 34 Ω). Comparison of small-signal parameters obtained by Monte Carlo (default setting), corner (FF, SS, FS, and SF), and temperature variation analyses are summarized in Table I.

B. DC Analysis of DVCC

Dynamics and linearity of the device was analyzed by applying DC sweep voltages or current at proper input terminals Y_1, Y_2, and X in order to evaluate both voltage and current transfer characteristics $Y_{1,2} \rightarrow X$ and $X \rightarrow Z$. Input voltage at Y_1 (or Y_2) was changed in range ±0.5 V and tested for Monte Carlo mismatch analysis and corner analysis. Selected results are depicted in Fig. 5. For both voltage transfers $Y_{1,2} \rightarrow X$ the limitations in dynamics are about ±400 mV and results yield maximal DC matching input offset approx. ±18 mV. Figure 5 also shows the result of DC transfer response for $X \rightarrow Z$ when sweeping an input current to X terminal in range ±500 µA, while $Y_{1,2}$ terminals were grounded. The obtained maximal DC current offset is approx. ±25 µA.

TABLE II. Main Small-Signal Parameters of the DVCC.

Parameter	Monte Carlo Analysis	Corner Analysis	Temperature Analysis
R_X [Ω]	31 – 34	24 – 44	28 – 33
$R_{Y1,2}$ [GΩ]	13.5	6.6 – 19	5 – 21
$C_{Y1,2}$ [fF]	118	84 – 242	77 – 314
R_Z [kΩ]	133 – 170	107 – 262	153 – 207
C_Z [fF]	16 – 180	155 – 199	155 – 173

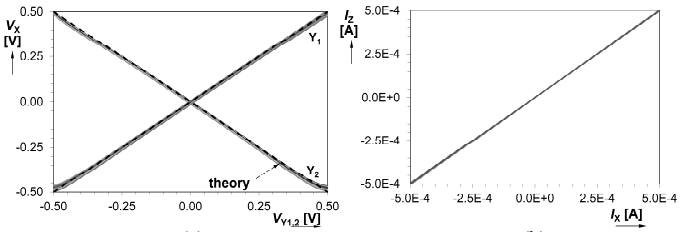

Fig. 5. Monte Carlo mismatch variation of DC transfer responses (100 runs): (a) $V_{Y1,2} \rightarrow V_X$, (b) $I_X \rightarrow I_Z$.

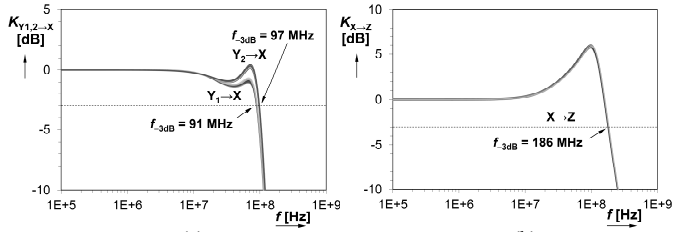

Fig. 6. Monte Carlo mismatch variation of AC transfer responses (100 runs): (a) $V_{Y1,2} \rightarrow V_X$, (b) $I_X \rightarrow I_Z$.

C. AC Analysis of DVCC

Corner effects are significant for AC behavior of designed DVCC due to direct effect on absolute values of compensation RC networks in CMOS implementation (Fig. 4). Magnitude responses of both voltage $Y_{1,2} \rightarrow X$ and current $X \rightarrow Z$ transfers are shown in Fig. 6. Voltage transfer characteristics indicate cut-off (–3 dB) frequencies from 91 MHz to 97 MHz in Monte Carlo mismatch analysis, however, in corner analysis dispersion is wider (from 55 MHz to 93 MHz). The same analysis was performed for current transfer and bandwidth are

supposed about 186 MHz and between 155 MHz and 195 MHz for Monte Carlo analysis and process corner deviations, respectively. Therefore, the maximum operating frequency of the DVCC according to Monte Carlo mismatch analysis is $f_{max\_MC} \ll \min\{1/\tau_{\gamma}, 1/\tau_{\beta j}\} \approx 91$ MHz, while the obtained frequency limitation of the proposed DVCC in corner analysis was $f_{max\_corner} \ll \min\{1/\tau_{\gamma}, 1/\tau_{\beta j}\} \approx 55$ MHz. For low-frequency region gains γ_o and β_{oj} are constants with values $1 - \varepsilon_{\gamma i} = 0.9998$, $1 - \varepsilon_{\beta 1v} = 0.99972$, $1 - \varepsilon_{\beta 2v} = 0.99972$. Hence, obtained errors of gains are low and can be expressed as $\varepsilon_{\gamma i} = 20 \cdot 10^{-3}$ and $\varepsilon_{\beta 1v} = \varepsilon_{\beta 2v} = 28 \cdot 10^{-3}$.

D. Verification of Integer-Order All-Pass Filter

The proposed pseudo-differential voltage-mode first-order all-pass filter shown in Fig. 2 was simulated in Cadence IC6 Spectre using designed DVCC shown in Fig. 4 and its input circuitry was used as VB ($V_X = V_{Y1}$, while V_{Y2} was grounded). Passive element values were selected as $R = 1$ kΩ, $C = 100$ pF, which resulted in a –90° phase shift at pole frequency $f_p = 3.18$ MHz. The ideal and simulated phase and gain responses are shown in Fig. 7(a) and (b). The obtained f_{p_sim} is 2.81 MHz. Note that the difference between simulation and theoretical values is due to non-idealities of the DVCC. Time-domain simulation results are shown in Fig. 7(c) in which a sine-wave input of 100 mV amplitude and frequency of f_{p_sim} was applied to the filter. The total harmonic distortion (THD) was found as 0.13%. The –90° phase shift in the output against the input at f_{p_sim} is illustrated by the Lissajous pattern shown in Fig. 7(d). Figure 8 shows the frequency spectrum of the output waveform with applying Hanning window. Computed Cadence IC6 Spectre simulation results are in good agreement with theory.

E. Verification of Fractional-Order All-Pass Filter

MAPLE plot given in Fig. 9 shows the effect of FoC order in range $\alpha = \{0.1 \text{ to } 1\}$ on magnitude (see Table I(a)) of the filter while $C_\alpha = C \cdot \omega^{1-\alpha}$. Subsequently, performance of the filter of order $\alpha = 0.8$ was further investigated in Cadence IC6 Spectre. Foster II RC network realization from Fig. 3 providing 4th-order approximation of FoC has been employed, which having a pseudo-capacitance value $C_{0.8} = 2.81$ nF/s$^{0.2}$ ($C = 100$ pF @f_{p_sim}). Computed component values using the continued fraction expansion method are given in Table III. Simulated phase and gain responses vs. frequency of the filter are compared with integer-order one in Fig. 7. As it can be observed, the deviation in gain of integer-order APF caused by real behavior of DVCC was compensated, while the phase shift @f_{p_sim} remained close to –90°. Similarly, comparison of time-domain simulations and frequency spectrum are given in Fig. 8. Considering same setup above (section III.D.), obtained THD value of the output waveform yields 0.14 %.

TABLE III. COMPONENT VALUES USED IN FIG. 3 FOR CADENCE SIMULATIONS APPROXIMATING $C_{0.8} = 2.81$ nF/s$^{0.2}$.

Values	R_0 [kΩ]	R_1 [Ω]	C_1 [pF]	R_2 [Ω]	C_2 [pF]	R_3 [kΩ]	C_3 [pF]	R_4 [kΩ]	C_4 [pF]
$\alpha = 0.8$	31.6	10.5	59	590	24.9	2.37	27.4	6.19	53.6

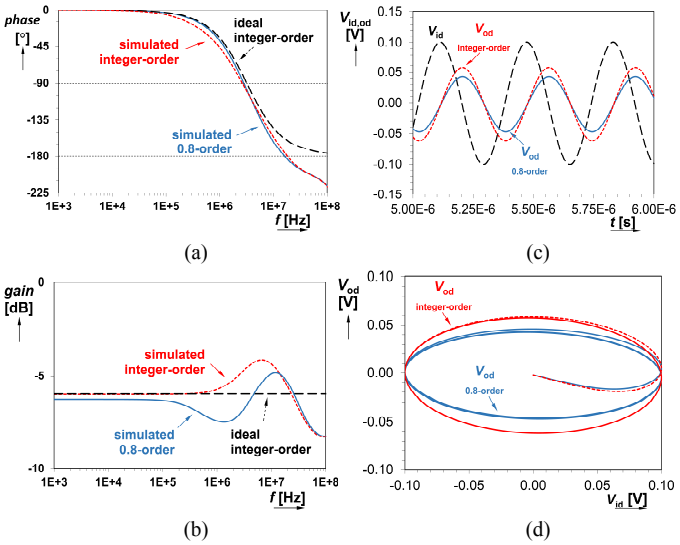

Fig. 7. Ideal and simulated (a) phase and (b) gain responses, (c) time-domain responses, (d) Lissajous pattern showing –90° phase shift of output against input voltage at f_{p_sim} of the P-D VM APF of orders $\alpha = [0.8; 1]$.

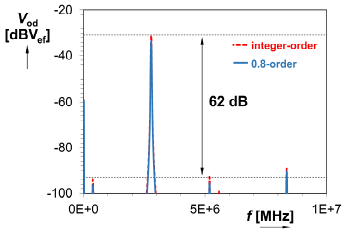

Fig. 8. Simulated frequency spectrum of the output of pseudo-differential VM APF of orders $\alpha = [0.8; 1]$.

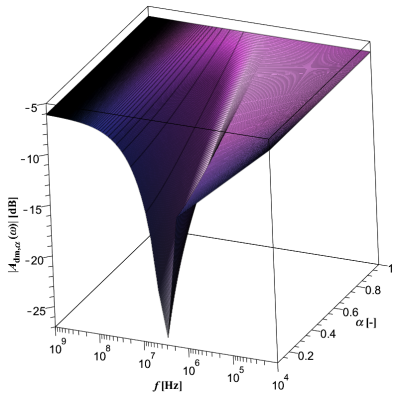

Fig. 9. Effect of α vs. frequency on magnitude of the P-D VM APF.

IV. CONCLUSION

The paper presented a novel structure of a pseudo-differential voltage-mode first-order all-pass filter employing an external resistor connected to low-impedance terminal of the designed high-performance CMOS DVCC and one grounded capacitor. Cadence IC6 Spectre simulation results confirmed the feasibility of the proposed filter. In addition, it was shown that a fractional-order capacitor can be used for gain response compensation of an all-pass filter. In the future work the introduced new application area of fractional-order capacitors will be further investigated.

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